Name _____

EE 2700 Exam 1. Spring 2012. 6 Pages. Open book, Open Notes. No Internet. Cheating will result in a score of 0 for this exam.

1. (4pts) Convert the following decimal numbers to 8-bit 2's complement numbers. Show your work.

(a) 91 (b) -107

2. (4 pts) Convert the following 8-bit 2's complement numbers to decimal (show your work).

(a) 11011011 (b) 01111001

3. (3 pts) Convert the following hexadecimal numbers to binary.

(a) C6 (b) 9BE (c) 5DF

4. (4 pts) Add or subtract the following 8-bit 2's complement numbers. State whether or not overflow has occurred (i.e. whether or not the result cannot be represented as an 8-bit 2's complement number).

(a) 10110011
+11010111

(b) 10010110
-01011011

5. (3 pts) Multiply the following two binary numbers and convert the result to decimal. When adding more than two binary numbers, add them two at a time. Show all work.

(a) 1101
×1011

6. (16 pts) Loop and give the simplest SOP (sum of products) expression for each of the following Karnaugh maps:

(a)

CD \ AB	00	01	11	10
00	1	1	0	1
01	0	0	1	0
11	0	0	0	0
10	1	1	0	1

F = _____

(b)

CD \ AB	00	01	11	10
00	0	0	0	0
01	1	1	0	1
11	0	1	1	1
10	0	0	0	0

F = _____

(c)

CD \ AB	00	01	11	10
00	1	x	1	x
01	0	1	x	x
11	0	x	0	0
10	1	x	1	x

F = _____

(d)

CD \ AB	00	01	11	10
00	$\bar{E}$	1	$\bar{E}$	xE
01	xE	xE+$\bar{E}$	x$\bar{E}$	0
11	0	E	x	1
10	xE+$\bar{E}$	E+ x$\bar{E}$	0	0

F = _____

7. (4 pts) Use the Karnaugh map on the right to simplify the following expression:

$$F = AB\bar{C} + \bar{A}BD + BCD + ABC\bar{D}$$

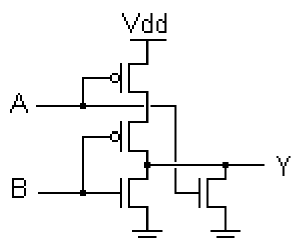
F = ______________________________

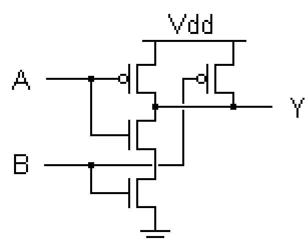
CD \ AB	00	01	11	10
00				
01				
11				
10				

8. (10 pts) Name the identity, property or theorem that justifies each of the following:

$A\bar{B}C + A\bar{B}C = A\bar{B}C$	*Identity X+X = X*
$A\bar{B}\bar{C} + AB\bar{C} = A\bar{C}$	______________________
$\bar{A}\bar{B}C + \bar{B}C = \bar{B}C$	______________________
$\bar{A} + \bar{B} + \bar{C} = \overline{ABC}$	______________________
$A + BC = (A + B)(A + C)$	______________________
$(A + B)(\overline{A + B}) = 0$	______________________

9. (4 pts) Name the standard logic gate (AND, NAND, OR or NOR) implemented by each of the circuits below: Hint: Transistors with bubbles are "on" when their gates (inputs) are low. Transistors without bubbles are "on" when their gates are high.

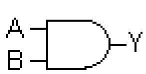




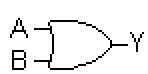
(a) ____________Gate

(b) __________ Gate

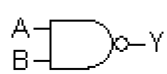
10. (4 pts) Complete the function tables for the logic devices shown below.



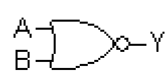
A	B	Y
L	L	
L	H	
H	L	
H	H	



A	B	Y
L	L	
L	H	
H	L	
H	H	



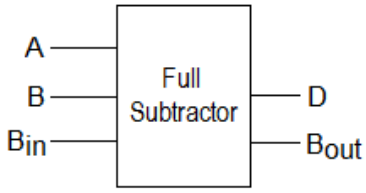
A	B	Y
L	L	
L	H	
H	L	
H	H	



A	B	Y
L	L	
L	H	
H	L	
H	H	

11. A full subtractor is like a full adder, except that it computes D = A – B – B_{in} and generates B_{out} if there is a borrow (rather than computing S = A + B + C_{in} and generating C_{out} if there is a carry).

(a) (4 pts) Complete the truth table for the full subtractor, below:



A	B	B_{in}	B_{out}	D
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

(b) (4 pts) Draw the Karnaugh maps for B_{out} and D. Group the maps to show that:

$$B_{out} = \bar{A}B_{in} + \bar{A}B + BB_{in} \text{ and } D = \bar{A}\bar{B}B_{in} + \bar{A}B\overline{B_{in}} + A\bar{B}\overline{B_{in}} + ABB_{in}$$

(c) (6 pts) Design a digital circuit using only NAND gates and inverters to implement the full subtractor. Assume all inputs and outputs are active high.

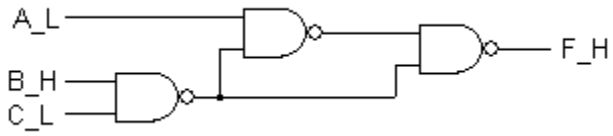
(d) (4 pts) Assume the following propagation delays: inverters, 3ns; 2-input gates, 4.5ns; 3-input gates, 5.5ns and 4-input gates, 6.5ns. Find the maximum propagation delay for outputs (a) B_{out} and (b) D.

(a) _____ (b) _____

12. (8 pts) Design a sum-of-products implementation of the function shown in the Karnaugh map below using only NAND or NOR gates. Inverters may be used on the inputs but not on the output. Assume A_H, B_H, C_L_ and F_L.

C \ AB	00	01	11	10
0	1	0	1	X
1	0	X	1	0

13. (4 pts) Analyze the circuit below to find an expression for F in terms of A, B and C. Express your answer as a sum of products. It is not necessary to reduce your answer to simplest form.



F = _____

14. Your first job out of college is to help design a universal battery charger for Dewalt. The charger senses whether the battery pack is 12 volts or 18 volts and charges it accordingly. Your job is to control the "charged" LED, which should come on at 12.0 volts for a 12V battery and 18.0 volts for an 18V battery. Fortunately, you have two signals, V12 and V18, both active (asserted) high that indicate that the battery voltage is at least 12.0 volts and 18.0 volts respectively. You also have signal B18 (active low) that indicates that an 18V battery is attached. Your output signal, CHARGED, is active low.

a) (4 pts) Finish the truth table below. To get full credit, you must use "don't cares" (X) where appropriate.

V18	V12	B18	CHARGED
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

b) (4 pts) Draw a Karnaugh map for the truth table in part (a) and find the simplest SOP expression for CHARGED.

CHARGED = _____

c) (6 pts) Design a digital circuit to implement the expression you found in part (b). Use only NAND or NOR gates. Inverters may be used on the inputs (rail) only. Remember that V12 and V18 are active high while B18 and CHARGED are active low.

Extra Credit (4 pts, no partial credit): Design another circuit for problem 14 using only an OR gate and a NAND gate. Hint: you will have to find a POS (product-of-sums) expression for CHARGED.